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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,008	03/23/2001	Richard E. Pekkala	BAN:0107	5720

23669 7590 02/09/2007
HUFFMAN LAW GROUP, P.C.
1900 MESA AVE.
COLORADO SPRINGS, CO 80906

EXAMINER	
DOAN, DUYEN MY	
ART UNIT	**PAPER NUMBER**
2152	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	02/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 02/09/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO@HUFFMANLAW.NET

Office Action Summary	Application No.	Applicant(s)	
	09/817,008	PEKKALA ET AL.	
	Examiner	Art Unit	
	Duyen M. Doan	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-113* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-113* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/14/06 has been entered. Claims 1-82 are amended for examination. Claims 83-113 are newly added.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-113 rejected under 35 U.S.C. 102(e) as being anticipated by Pettey et al (us pat 6,594,712) (hereinafter Pettey).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As regarding claim 1, Pettey discloses a plurality of media access controllers (MACs), for transceiving packets (see col.7, lines 29-38, plurality of MACs); a local bus interface, for performing addressed data transfers on a local bus coupled thereto (col.7, lines 40-44); a bus router, for performing transport layer operations between said plurality of MACs and said local bus interface (col.7, lines 66-67; col.8, lines 1-7, also see figure 3, bus router 306); a memory, shared by said plurality of MACs, said local bus interface, and said bus router, for buffering data received thereby (see col.8,lines 37-67, also see Fig.3, memory blocks 304); and a transaction switch, coupled to each of said memory, said plurality of MACS, said local bus interface and said bus router, for switching data and transactions therebetween (see col.8, lines 8-36, also see figure 3 switch 202).

As regarding claim 2, Pettey discloses a plurality of transaction queues, associated with said plurality of MACs, said local bus interface, and said bus router, coupled to said transaction switch, for storing said transaction (see col.11, lines 8-26).

As regarding claim 3, Pettey discloses a random access memory (see col.8, lines 21-36).

As regarding claim 4, Pettey discloses a buffer manager, for allocating portions of said memory to said plurality of MACs, said local bus interface and said bus router, for buffering said data received thereby (see col.8, lines 21-67)

As regarding claim 5, Pettey discloses buffer manager performs said allocating in an as-needed manner (see col.16, lines 25-41).

As regarding claim 6, Pettey discloses said bus router is configured to write packet header into said memory via said transaction switch along with addressed data stored in said memory by said local bus interface to create packet (see col.14, lines 10-54).

As regarding claim 7, Pettey discloses local bus interface configured to read a payload portion of packet stored in said memory and to transmit said payload portion on said local bus coupled thereto (see col.18, lines 14-37).

As regarding claim 8, Pettey discloses said payload portion is located in said memory at an offset specified in a transaction posted by said bus router to said local bus interface via said transaction switch (see col.18, lines 14-51).

As regarding claim 9, Pettey discloses wherein said local bus interface comprises a PCI interface (see col.18, lines 14-18).

As regarding claim 10, Pettey discloses transaction switch is configured to receive a transaction posted by a first of said plurality of MACs in response to a packet received by said first of said plurality of MACs and to selectively witch said transaction to one of a second of said plurality of MACs and said bus router (see col.8, lines 8-36).

As regarding claim 11, Pettey discloses transaction switch selectively switches said transaction based on an Infiniband destination local identification value included in said transaction (see col.8, lines 8-36).

As regarding claim 12, Pettey discloses transaction switch selectively switches said transaction to said bus router if an entry associated with said InfiniBand destination local identification value in a mapping table of said transaction switch indicates said transaction is destined for said bus router (see col.8, lines 8-36).

As regarding claim 13, Pettey discloses said transaction switch selectively switches said transaction to one of said plurality of InfiniBand MACs based on which of said plurality of InfiniBand MACs is associated with said InfiniBand destination local identification value in said mapping table if said entry indicates said transaction is not destined for said bus router (see col.8, lines 8-36; col.14, lines 1-54).

As regarding claim 14, Pettey discloses first MAC parses said InfiniBand destination local identification value from said packet (see col.8, lines 8-36; col.14, lines 1-54).

As regarding claim 15, Pettey discloses transaction includes an InfiniBand virtual lane number parsed from said packet (see col.9, lines 1-33).

As regarding claim 16, Pettey discloses transaction includes a destination queue pair number parsed from said packet (see col.9, lines 1-33).

As regarding claim 17, Pettey discloses transaction switch is configured to receive a transaction posted by said bus router and to selectively switch said

transaction to one of said plurality of MACs and said local bus interface (see col.14 lines 10-65).

As regarding claim 18, Pettey discloses transaction switch selectively switches said transaction based on a transaction type value included in said transaction (see col.14 lines 10-65).

As regarding claim 19, Pettey discloses a second local bus interface for performing addressed data transfers on a second local bus coupled thereto; wherein said transaction switch selectively switches said transaction to one of said first and second local bus interfaces based on whether a local bus address included in said transaction falls into one or more predetermined address ranges of said first and second buses (see figure col.14, lines 10-54).

As regarding claim 20, Pettey discloses said transaction includes an address in an address range of said local bus (see col.9, lines 14-43).

As regarding claim 21, Pettey discloses a second local bus interface for performing addressed data transfers on a second local bus coupled thereto (see col.9, lines 14-43); a local bus bridge coupled between said first and second local bus interfaces for buffering data therebetween (see col.9, lines 14-43).

As regarding claim 22, Pettey discloses a second bus interface; wherein said transaction switch is configured to receive a transaction posted by said first local bus interface in response to an addressed data transfer received by said first local bus interface and to switch said transaction to second local bus interface (see col.9, lines 14-60).

As regarding claim 83, Pettey discloses wherein at least one of said plurality of MACs comprises an Infiniband MAC (see col.7, lines 29-44).

As regarding claim 83, Pettey discloses wherein at least one of said plurality of MACs comprise an Ethernet MAC (see col.7, lines 29-44).

As regarding claim 93, Pettey discloses wherein at least one of said plurality of addressed data devices comprises an interface to a bus for coupling to a random access memory (see col.8, lines 21-36).

As regarding claim 23, Pettey discloses a memory, shared by the plurality of data devices for buffering data received thereby (see col.8, lines 37-67, also see figure 3, share memory 304); multiplexing logic, for controlling the transfer of data between the plurality of data devices and said memory (col.8, lines 37-67, also see figure 3, switch); and control logic, for controlling said multiplexing logic; wherein the plurality of data devices comprise a plurality of packetized data devices and a plurality of addressed data devices (see col.7, lines 29-67; col.8, lines 1-36); wherein said control logic is configured to selectively control said multiplexing logic to transfer data through said memory between two of said packetized data devices and between one of said packetized data devices and one of said addressed data devices (see col.7, lines 29-67; col.8, lines 1-36).

As regarding claim 24, Pettey discloses wherein said control logic is further configured to selectively control said multiplexing logic to transfer data through said memory between two of said addressed data devices (see col.7, lines 29-67; col.8, lines 1-36).

As regarding claim 25, Pettey discloses wherein said control logic is configured to selectively control said multiplexing logic to transfer data through said memory between two of said packetized data devices and between one of said packetized data devices and one of said addressed data devices concurrently (see Abstract).

As regarding claim 26, Pettey discloses wherein at least two of said packetized data devices comprise InfiniBand interfaces (see col.7, lines 29-67; col.8, lines 1-36).

As regarding claim 27, Pettey discloses wherein at least two of said addressed data devices comprise PCI bus interfaces (see col.7, lines 29-67; col.8, lines 1-36).

As regarding claim 28, Pettey discloses a buffer manager, for allocating portions of said memory to the plurality of data devices for buffering said data (see col.7, lines 29-67; col.8, lines 1-36).

As regarding claim 29, Pettey discloses wherein buffer manager is configured to perform said allocating on substantially a first-come-first-serve basis (see col.16, lines 24-60).

As regarding claim 30, Pettey discloses said control logic is configured to selectively control said multiplexing logic to transfer data through said memory between two of said packetized data devices and between one of said packetized data devices and one of said addressed data devices in response to a transaction posted to the transaction switch by the plurality of data devices (see col.8, lines 8-36; col.14, lines 1-54).

As regarding claim 31, Pettey discloses transaction comprises a command to transfer data between said memory and one of the plurality of data devices (see col.8, lines 8-36; col.14, lines 1-54).

As regarding claim 32, Pettey discloses wherein said transaction comprises an address of a buffer within said memory wherein is stored said data to be transferred in (see col.8, lines 8-36; col.14, lines 1-54).

As regarding claim 33, Pettey discloses transaction comprises an offset within said buffer for addressing portions of said data (col.18, lines 14-51).

As regarding claim 34, Pettey discloses wherein said transaction comprises a tag for uniquely identifying said transaction from other transactions posted to the transaction switch by the plurality of data devices (col.18, lines 14-51).

As regarding claim 35, Pettey discloses wherein the plurality of data devices comprise a transport layer device, wherein the transaction switch is configured to receive transactions from said transport layer device for performing protocol translation of data between said one of said packetized data devices and said one of said addressed data devices (col.18, lines 14-51).

As regarding claim 80, Pettey discloses wherein a single integrated circuit comprises the transaction switch (see figure 3).

As regarding claim 85, Pettey discloses wherein at least one of said at least two of said packetized data devices comprises an Ethernet interface (see col.6, lines 39-46).

As regarding claim 94, Pettey discloses wherein at least one of said plurality of addressed data devices comprises an interface to a bus for coupling to a random access memory (see col.8, lines 21-36).

As regarding claims 36-40,81,86,95, limitations are similar to limitations of rejected claims 23-35,80,85,94, therefore rejected for the same rationale.

As regarding claims 41-62,87,96, the limitations are similar to limitations of rejected claims 1-22,83-84,93, therefore rejected for the same rationales. Pettey further discloses at least three interfaces, and at least one of said at least three data interfaces is of a different type that the others (see figure 3, PCI interface316, PCI interface 312, bus router, MACs).

As regarding claims 63-66,88-89,97, the limitations are similar to limitations of rejected claims 41-62,87,96, 83 therefore rejected for the same rationales.

As regarding claims 67-70,82,90-91,98, the limitations are similar to limitations of rejected claims 1-22,83-84,93, therefore rejected for the same rationales.

As regarding claims 71-78,92,99, the limitations are similar to limitations of rejected claims 1-22,83-84,93, therefore rejected for the same rationales.

As regarding claim 79, the limitations are similar to limitations of rejected claims 23-65,80,85,94, therefore rejected for the same rationale.

As regarding claim 100, Pettey discloses invention substantially as claimed in claim 1, Pettey further discloses wherein the transport protocol engine is configured to perform the protocol translation before the MAC reads the packet from the memory for transmission on the network, wherein the transport protocol engine performs the

protocol translation without copying the data to another memory (see abtract, col.4, lines 30-67; col.9, lines 6-12).

As regarding claim 101, Pettey discloses wherein the transport protocol engine is further configured to perform second protocol translation from the packetized data protocol to the addressed data protocol by identifying a data payload within a second packet received from the network by the MAC and specifying a local bus address for the data payload (see col.4, lines 30-67; col.8, lines 36-67; col.9, lines 6-12; col.14, lines 10-60); wherein the transport protocol engine is further configured to perform the second protocol translation before the local bus interface reads the data payload from the memory for writing on the local bus to the local bus address, wherein the transport protocol engine performs the second protocol translation within the memory without copying the data to another memory (see col.4, lines 30-67; col.8, lines 36-67; col.9, lines 6-12; col.14, lines 10-60).

As regarding claim 102, Pettey discloses wherein a single integrated circuit comprises the local bus interface, the MAC, the transport protocol engine, the memory, and the transaction switch (see figure 3).

As regarding claim 103, Pettey discloses wherein the transport protocol engine is configured to create the packet by writing a packet header into the memory in front of the data (col.14, lines 10-60).

As regarding claims 104-107, the limitations are similar to limitations of claims 100-103, therefore rejected for the same rationale as claims 100-103.

As regarding claim 108, Pettey discloses allocating by the transaction switch a portion of the memory for buffering data received on the local bus by the local bus interface (see col.7, lines 40-65; col.8, lines 8-36; col.18, lines 14-51; col.19, lines 4-35); writing, by the local bus interface, the data into the allocated portion of the memory creating, by the transport protocol engine, with the data a packet within the allocated portion of the memory (see col.7, lines 40-65; col.8, lines 8-36; col.18, lines 14-51; col.19, lines 4-35); and reading, by the MAC, the packet from the allocated portion of the memory for transmission on a network, after said creating, wherein the transport protocol engine performs said creating the packet without copying the data to another memory (see col.7, lines 40-65; col.8,lines 8-36; col.18, lines 14-51; col.19, lines 4-35).

As regarding claim 109, Pettey discloses allocating, by the transaction switch, a second portion of the memory for buffering a second packet received from the network by the MAC (see col.7, lines 40-65; col.8, lines 8-36; col.18, lines 14-51; col.19, lines 4-35); writing, by the MAC, the second packet into the second allocated portion of the memory (see col.7, lines 40-65; col.8, lines 8-36; col.18, lines 14-51; col.19, lines 4-35); identifying, by the transport protocol engine, a data payload within the second packet (see col.7, lines 40-65; col.8,lines 8-36; col.18, lines 14-51; col.19, lines 4-35); specifying, by the transport protocol engine, a local bus address for the data payload (see col.7, lines 40-65; col.8,lines 8-36; col.18, lines 14-51; col.19, lines 4-35); and reading, by the local bus interface, the data payload from the second allocated portion of the memory for writing on the local bus to the local bus address, after said identifying and said specifying, wherein the transport protocol engine performs said identifying and

said specifying without copying the data to another memory (see col.7, lines 40-65; col.8,lines 8-36; col.18, lines 14-51; col.19, lines 4-35).

As regarding claim 110, Pettey discloses wherein the transport protocol engine is configured to create the packet by writing a packet header into the memory in front of the data (col.14, lines 10-60).

As regarding claims 111-113, the limitations are similar to limitations of rejected claims 108-110, therefore rejected for the same rationale.

Response to Arguments

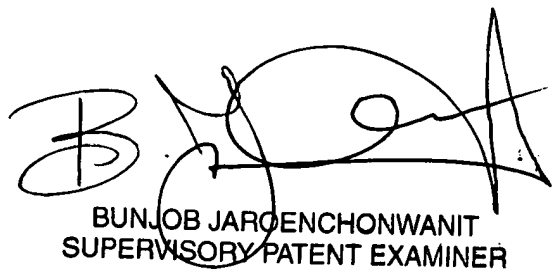
Applicant's arguments with respect to claims 1-113 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duyen M. Doan whose telephone number is (571) 272-4226. The examiner can normally be reached on 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on (571) 272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Duyen Doan
Art unit 2152



BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER